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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,306	11/04/2003	Hea Suk Jung	CU-3424 WWP	5038

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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/701,306	JUNG, HEA SUK	
	Examiner	Art Unit	
	KHAREEM E. ALMO	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al. (US 7088797)

With respect to claim 1, Figures 9 and 10 of Momtaz et al. disclose a synchronous memory device for synchronization of an external input clock (REFCLK) with an internal input clock (VNCLK) comprising: a Phase locked loop having a clock divider (901) comprising a plurality of clock signal dividers (911 and 912) connected in series, a power down controller (202) for determining a power down condition based at least on a predetermined state of a clock enable signal (add or drop) that controls whether the memory device receives the external input clock and that is inputted to the loop, wherein the clock divider outputs a first clock signal (at the output of 912) being one of the output signals of the clock signal dividers excluding the last clock signal divider (912) of the series when the synchronous memory device is in the a non power down condition (Note: the power down condition is determined by the user to output a "power down signal" determined by the user when a certain sequence occurs") , wherein the clock divider (901) outputs a second clock signal (between 911 and 912) being an output signal of the last clock signal divider of the series when the

synchronous memory device is in a power down condition (Note: the power down condition is determined by the user to output a "power down signal" determined by the user when a certain sequence occurs"), and wherein a frequency of the first clock signal is higher than that of the second clock signal but fails to disclose the Phase locked loop being a (DLL). It is well known in the art to include a deskew PLL on the receive side so that the clock at each data flip-flop is phased-matched to the received clock (i.e. use a DLL in the place of an PLL). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a deskew PLL on the receive side so that the clock at each data flip-flop is phase matched to the received clock for the well known purpose of eliminating delay limits in the frequency at which data can be sent.

With respect to claim 15, the circuit above produces the synchronous memory device of claim 14, wherein the frequency of the first clock signal is 2M when the frequency of the second clock signal is M. (Note this claim is met because the dividing ratio can be selected by the user so that the first clock signal frequency is M and the second clock signal frequency is 2M (see chart in figure 10)).

Response to Arguments

3. Applicant's arguments filed 4/30/2010have been fully considered but they are not persuasive.

With respect to applicant's argument that Momtaz fails at least to disclose the clock enable signal and the power down condition of the presently claimed invention, the Examiner disagrees.

Applicant argues that a power down condition is a mode in which power is saved, the Examiner disagrees. A power down condition is any condition that determines the status of power down. The power down controller does not have to power down the device, but merely has to control a power down condition. If the condition is not powered down, that condition is still a power down condition.

Applicant further argues that the add/drop of Momtaz is generated by detecting the number of data bits while the data input/operations are performed and do not control whether the an external input clock is received and therefore unlike the claimed clock enable signal, the Examiner disagrees. As shown in figure 10 of Momtaz, the add drop signals determine if the REFCLK is enabled based on predetermined conditions (00, 01,10 and 11). As shown in figure 10, a predetermined state conditions (00, 01,10 and 11) of a clock enable signal (add or drop)

ADD	DROP	F_{OUT}
0	0	$F_{IN}/2$
0	1	$F_{IN}/4$
1	0	F_{IN}
1	1	$F_{IN}/2$

FIG. 10

controls whether the memory device receives the external input clock signal (when add is 1 and drop is 0 FIN is output (FIN would be REFCLK), thus determines whether the Fin (REFCLK) goes through the MUX, therefore controls whether the memory device downstream receives the signal)

Claim 15 is rejected for similar reasons above.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1736. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khareem E Almo/
Examiner, Art Unit 2816
/Lincoln Donovan/
Supervisory Patent Examiner, Art Unit 2816